ERROR CORRECTION FOR PROGRAMMABLE LOGIC INTEGRATED CIRCUITS

[0075] Systems and methods for detecting and correcting errors in programmable logic ICs are provided. In one embodiment, a scrubber periodically reads the memory cells in a programmable logic IC, detects and corrects any errors, and writes the corrected contents back into the memory cell. In another embodiment, regions of memory cells in a programmable logic IC each have associated error correcting circuitry which operates to continuously detect and correct errors as they occur. Error correcting circuitry can further be designed to reduce static hazards. It may be more desirable to design programmable logic IC routing architectures that reduce the number of memory cells needed to implement a given function. Error correcting circuitry can be provided for configuration memory or for an embedded memory block on a programmable logic IC.